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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MORTEZA CYRUS AFGHAHI and ESIN TERZIOGLU

Appeal 2011-006666
Application 10/795,825
Technology Center 2800

Before MAHSHID D. SAADAT, JOHN A. JEFFERY, and
ELENI MANTIS MERCADER, *Administrative Patent Judges*.

MANTIS MERCADER, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants seek our review under 35 U.S.C. § 134 of the Examiner's rejection of claims 9 and 10. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

INVENTION

Appellants' claimed invention is directed to a single-ended sense amplifier having a DataIn voltage sampled and stored as a reference voltage at node 1021 just before a measurement is taken, thereby making the circuit substantially independent of ground or supply voltage references (Spec. 34:5-15).

Claim 9, reproduced below, is representative of the subject matter on appeal:

9. A method of measuring an input signal using a single-ended sense amplifier, the method comprising:

sampling a voltage present at an input node a predetermined interval before measurement of the input signal is initiated;

holding the sampled voltage at a reference node as a reference voltage; and

at the predetermined interval after sampling the voltage present at the input node, measuring the input signal at the input node by sampling the input signal and comparing it to the reference voltage.

THE REJECTION

The Examiner relies upon the following as evidence of unpatentability:

Kerth	US 5,477,481	Dec. 19, 1995

The following rejection is before us for review:

Claims 9 and 10 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kerth.

ISSUE

The issue is whether the Examiner erred in finding that Kerth teaches the limitation of "measuring the input signal at the input node by sampling the input signal and *comparing it to the reference voltage*" as recited in claim 9 (emphasis added).

PRINCIPLE OF LAW

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros., Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987).

ANALYSIS

Kerth's Figure 4A is depicted below:

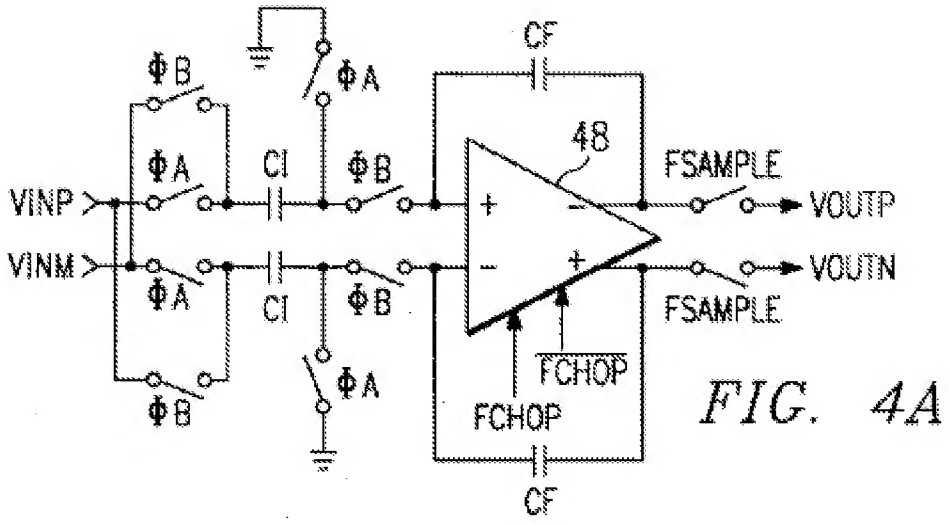

FIG. 4A

Kerth's Figure 4A shows a differential amplifier 48 wherein the switches are open or closed depending on the timing signals ϕA and ϕB.

Kerth's Figure 1C is depicted below:

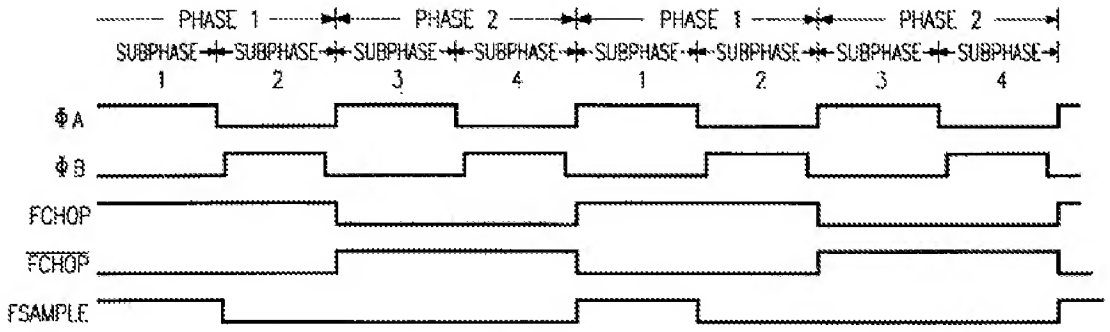

FIG. 1C

Kerth's Figure 1C shows the timing signals ϕA and ϕB which Figure 4A applies (col. 7, ll. 35-39).

The Examiner asserts

> the input signal VINP gets compared to the reference voltage via comparator 48 (i.e., when the switches [ϕ]B close, the sampled and held voltage on the top capacitor CI gets applied to the non-inverting input terminal of comparator 48 and *the input signal VINP gets applied to the inverting input terminal of comparator 48*).

(Ans. 6 (emphasis added)).

We do not agree with the Examiner's assertion. At the outset, we note that the Examiner deems the "input node" of claim 9 to be the terminal receiving VINP, and the "reference node" to be the left terminal of top capacitor CI (Ans. 6).

Appellants noted that when the top switch ϕA is closed, the bottom switch ϕA is also closed (Reply Br. 2; *see also* Fig. 1C (Figure 4A follows the same timing principles as those indicated in Figure 1C); col. 5, ll. 4-6;

col. 7, ll. 35-39). Therefore, when the ϕA switches are closed and the ϕB switches are open ("subphase 1" in Fig. 1C of Kerth), signal VINP is stored at the left terminal of top capacitor CI and signal VINM is stored at the left terminal of bottom capacitor CI (Fig. 4A). When the ϕA switches are open and the ϕB switches are closed ("subphase 2" in Fig. 1C of Kerth), the signal at the left terminal of top capacitor CI (which the Examiner deems to be the "reference voltage" of claim 9) is passed to the positive input of amplifier 48. At the same time, the signal at the left terminal of bottom capacitor CI is passed to the negative input of amplifier 48. Thus, the Examiner's "reference voltage" (i.e., the signal stored at the top capacitor CI of Figure 4A) is compared, not to "the input signal" VINP, but rather, to the signal stored at the bottom capacitor CI of Figure 4A.

Thus, Appellants' argument has persuaded us of error in the Examiner's rejection of claim 9 and of claim 10 which depends from claim 9. Accordingly we will reverse the Examiner's rejection of claims 9 and 10.

CONCLUSION

Appellants have shown that the Examiner erred in finding that Kerth teaches the limitation of "measuring the input signal at the input node by sampling the input signal and comparing it to the reference voltage" as recited in claim 9.

ORDER

The decision of the Examiner to reject claims 9 and 10 is reversed.

REVERSED

babc